Extreme Soldering: You Can Do BGA

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What I’ll cover

1. Overview of BGA and surface mount
2. PCB design
3. Assembly / Rework
Package size evolution
No reason to be scared of BGA

- Much easier to assemble
- More compact
- Can use newer parts
- BUT, rework more difficult
What is BGA

- Popular package for CPUs, memory, SoCs, interface chips
- High pin count, small space
- Can be difficult to “break out”
- Necessary for modern fast digital

- Quick, cheap 4-layer services mean small BGAs are perfectly usable for prototyping
Variants of BGA packages

Overmolded wirebond

Cutaway diagrams © Amkor
Variants of BGA packages

Lidless flip chip
Variants of BGA packages

Lidded flip chip (heatspreader over die)
Footprint measurements

- Pitch
- Land size (usually function of pitch)
- Pattern (any voids)
- Total ball count

- Most packages have grid-aligned balls
- Horiz/vertical pitch may not be square
Typical metrics

- 0.5mm (Low ball count, PoP)
- 0.8mm (SoC, DDR)
- 1.0mm (Large FPGAs)
- 1.27mm (Legacy devices)
- Total balls can range from 4 to over 1000-2000
- Leaded balls, leadfree (RoHS)

- Larger pitches much easier to break out
PCB layout for BGA

- Can be done in just about any package
- I’ve used Eagle, Altium, others used Kicad
- Hand routing essential for layer count
- Footprints easy, symbols not
- Typical high speed layout rules apply
PCB specs required

- 4 layers is the sane minimum for most
- 256 balls possible on 4 layer
- 324 requires 6 layers
- 484 requires 8 layers
- For example a high end Stratix FPGA with ~1400 may take 16 layers
- ENIG, Immersion Silver
- PTH vs microvias
Layout process

- Fanout all pads except 2 outer rings
- Next two rings via’d to bottom layer
- Ground, power fills
- Land diameter: 2/3 of ball diameter
  - Example: 1.0mm bga
    - 0.8mm balls
    - 0.48mm land size

- 1.0mm:
  - 13mil drill, 21mil diameter, 6mil trace/space
- 0.8mm:
  - 10mil drill, 18mil diameter, 5mil trace/space
Outer two rings

Inner area

Ball land
Ball land styles

- **NSMD (Non-solder mask defined)**
  - Most common, allows solder to “grab” around copper

- **SMD (Soldermask defined)**
  - Used when not enough space
Pads over vias?

- DON’T!
- Result: via steals solder, stressing joint, outgassing causes voids

- Real via-in-pad (VIP):
  - Plugged vias
  - Capped vias

- Aids bypass caps, costs $$$
PCB Inspection

- 1. Soldermask-copper alignment
- 2. Ensure annular ring on all vias
- 3. Pad coplanarity
- 4. Plating
Assembly Overview

- Apply paste
- Place parts
- Reflow

- Process is critical!!
- BGAs come preballed (leadfree)
- Either paste, or just flux the pcb

- Placement of BGA is super simple and easy
- Alignment: Copper best
Sitting on paste (recommended)

Sitting on flux (A+ planarity needed)
Alignment less critical
Solder paste

- Buy quality; cheap paste sucks
- BGAs come with leadfree balls
- Good for 6mos
- Store in fridge, don’t freeze

- I use SMD291SNL10-ND
Stencils

- Kapton (3,5mil)
- Stainless steel

Soldertools.net
Oshstencils.com
Ohararp.com
Heating paste past melting temp consistently and holding for a bit

Exact timing/temps important for big runs

“Good enough” works for prototypes

Convection oven > skillet > hotair station
Reflow

- Hotair station only works for very small (<200 pin) monolithic BGA and QFNs
- Hotplate gives uneven heating, only 1 side
- Convection oven best bet
Reflow profiles

- Consult datasheets of the critical parts on PCB such as main processor, large connector etc
- Basically all the same depending
- Leadfree and leaded are different of course
- Always do dry run with a dummy pcb of same thermal mass
Figure 1. IR/Convection Reflow Profile (IPC/JEDEC J-STD-020D.1)

- T_p ≥ T_c (Supplier)
- T_p ≤ T_c (User)
- T_c - 5°C
- Max. Ramp Up Rate = 3°C/s
- Max. Ramp Down Rate = 6°C/s
- Time 25°C to Peak

Temperature

T_p

T_L

T_{smax}

T_{smin}

Preheat Area

Time

25°C
temperature

maximum peak temperature
= MSL limit, damage level

minimum peak temperature
= minimum soldering temperature

peak temperature

time

MSL: Moisture Sensitivity Level

001aac844
Reflow profiles

- Preheat ramp speed
- Soak time (deprecated for RoHS)
- Time above liquidus
- Cooldown speed (degrees/second)

For protos, exact rates not critical!
<video>
Failures

- Too long in soak will burn off flux
- Excessive voiding in solder balls
- Poor coplanarity of pads; bad wetting

Other failures can manifest in the field:
- Stress fractures caused by voids near joint
- Dendritic growth/tin whisker
- PCB failures such as via>plane shorts
- Thermal cycling stress
- Vibration/shock
Rework

- Most BGAs only rated to withstand 3 cycles
- Preheating is necessary
- Hard to heat joints by blasting the top of the package
R&R

- Remove BGA
- Site PCB prep
  - Clean pcb lands, must be flat
  - 99% isopropyl
- Prep BGA
  - Remove all solder
  - Isopropyl
  - Chip away flux residue again
  - Flux and place balls
  - Reflow in oven only
Further reading

- Altera reflow guidelines

- Intel process guidelines

- NXP reflow appnote

- Breakout out very large devices
Questions
Thanks

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